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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,011	02/02/2001	Takashi Tanimoto	2933SE-94	7450

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EXAMINER
TRA, ANH QUAN

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/776,011	TANIMOTO, TAKASHI	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6 and 9* is/are rejected.

7)☒ Claim(s) *4,5,7,8,10 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mukainakano et al. (USP 6107862).

As to claim 1, Mukainakano et al. shows in figure 7A a charge pump circuit comprising: a plurality of switching circuits (SW1, SW2) connected in series between an output terminal and reference potential terminal (V1) of the charge pump circuit, wherein the plurality of switching circuit includes a first switch (SW1) connected to the reference potential terminal and a second switch (SW2) connected to the first switch, and wherein the first switch has a control terminal provided with a first clock signal (B), and the second switch has a control terminal provided with a second clock signal (A), the first and second clock signals having inverted phases; a capacitor (C1) connected to a node between the first and second switches and having a first terminal and a second terminal; and a delay circuit (SW3, RSW3, SW4) connected between the second terminal of the capacitor and the control terminal of the first switch, wherein the delay circuit delays the first clock signal by a predetermined time and provides the delayed first clock signal to the second terminal of the capacitor. Thus, figure 7A shows all limitations of the claims except for the switching circuits are switching transistors. However, it is well known in the art that

transistor having equivalent function with the switch circuit. Therefore, it would have been obvious to one having ordinary skill in the art to replace the switching circuits with transistors due to doctrine equivalent function.

As to claim 2, figure 7A shows a buffer circuit (inverter providing signal B) functioning between a predetermined power supply potential and a potential at the node for receiving the first clock signal and providing a buffered clock signal to the delay circuit and the control terminal of the first transistor.

As to claim 3. figure 7A shows a timing adjustment circuit (pulse generator) connected to the buffer circuit to generate the first and second clock signals so that a period during which the first and second transistors are simultaneously deactivated exists.

As to claim 6, it is inherent that the delay circuit temporarily sets the second terminal of the capacitor in a high impedance state and, after delaying the first clock signal by the predetermined time from when the first clock signal is inverted, provides the delayed first clock signal to the second terminal of the capacitor.

As to claim 9, it is inherent that the delay circuit temporarily sets the second terminal of the capacitor in a high impedance state and, after delaying the first clock signal by the predetermined time from when the first clock signal is inverted, provides the delayed first clock signal to the second terminal of the capacitor.

Allowable Subject Matter

3. Claims 4, 5, 7, 8, 10 and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 4 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 3) having the timing adjustment circuit (10) includes: a first inverter (13) for receiving the delayed first clock signal, inverting the first clock signal, and generating an inverted first clock signal; a second inverter (12) for inverting an original clock signal provided to the charge pump circuit and generating an inverted original clock signal; a first NAND circuit (15) connected to the first and second inverters for receiving the inverted original clock signal and the inverted first clock signal to generate the second clock signal; a third inverter (11) for receiving the second clock signal and generating an inverted second clock signal; and a second NAND circuit (14) connected to the third inverter for receiving the original clock signal and the inverted second clock signal to generate the first clock signal.

Claim 5 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 5) having a timing adjustment circuit includes (20): a first NOR circuit (25) for receiving an original clock signal provided to the charge pump circuit and the second clock signal to generate a first NOR logic signal; a first inverter (23) connected to the first NOR circuit for inverting the first NOR logic signal and generating the first clock signal; a second inverter (21) for inverting the original clock signal and generating an inverted original clock signal; a second NOR circuit (24) connected to the second inverter for receiving the first clock signal and

the inverted original clock signal to generate a second NOR logic signal; and a third inverter (22) connected to the second NOR circuit for inverting the second NOR logic signal and generating the second clock signal.

Claims 7, 8, 10 and 11 would be allowable because the prior art fails to teach or suggest a circuit (such as figure 8) having a delay circuit (110) includes: third and fourth transistors (111, 113) connected in series between a high potential power supply and a low potential power supply, wherein a second node between the third and fourth transistors is connected to the second terminal of the capacitor; a first logic circuit (116, 117) for providing a first control signal to a control terminal of the third transistor; and a second logic circuit (115) for providing a second control signal to a control terminal of the fourth transistor, wherein one of the first and second logic circuits generates its control signal based on the first clock signal and the control signal of the other one of the first and second logic circuits so that a period during which the third and fourth transistors are simultaneously deactivated exists.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 703-308-6174. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

QT
February 5, 2002

Toan Tran
Primary Examiner